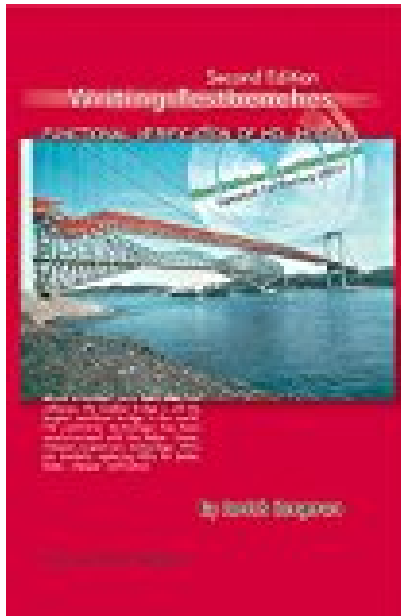


Writing Testbenches Functional Verification of HDL Models



BOOK DETAILS

- Author : Janick Bergeron
- Pages : 478 Pages
- Publisher : Springer
- Language : English
- ISBN : 1402074018



BOOK SYNOPSIS

mental improvements during the same period. What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough. In the second edition of *Writing Testbenches*, Bergeron raises the verification level of abstraction by introducing coverage-driven constrained-random transaction-level self-checking testbenches all made possible through the introduction of hardware verification languages (HVLs), such as e from Verity and OpenVera from Synopsys. The state-of-art methodologies described in *Writing Testbenches* will contribute greatly to the much-needed equivalent of a synthesis breakthrough in verification productivity. I not only highly recommend this book, but also I think it should be required reading by anyone involved in design and verification of today's ASIC, SoCs and systems. Harry Foster Chief Architect Verplex Systems, Inc. xviii *Writing Testbenches: Functional Verification of HDL Models*
PREFACE If you survey hardware design groups, you will learn that between 60% and 80% of their effort is now dedicated to verification.

WRITING TESTBENCHES FUNCTIONAL VERIFICATION OF HDL MODELS -

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